REMARKS

The present application was filed on February 20, 2002 with claims 1 through 20. Claims 1 through 20 are presently pending in the above-identified patent application.

In the Office Action, the Examiner rejected claims 1-2, 5, 7-8, 11, 13-14, 16, and 19 under 35 U.S.C. §102(e) as being anticipated by Kikuchi (United States Patent Number 6,606,715), rejected claims 3, 9, and 17 under 35 U.S.C. §103(a) as being unpatentable over Kikuchi in view of Hwu et al. (United States Patent Number 6,681,387), and rejected claims 4, 6, 10, 12, 15, 18, and 20 under 35 U.S.C. §103(a) as being unpatentable over Kikuchi in view of Borg et al. (United States Patent Number 5,274,811).

Independent Claims 1, 7, 13 and 16

Independent claims 1, 7, 13, and 16 were rejected under 35 U.S.C. §102(e) as being anticipated by Kikuchi. Regarding claim 1, the Examiner asserts that Kikuchi discloses determining a number (block count / boundary of data blocks) of live frames (blocks during execution) of said application that are coexistent during execution of said application (col. 11, lines 30-67); and establishing said bound based on said number of live frames (block count / boundary of data blocks) (col. 11, lines 30-67). In the Response to Arguments section of the final Office Action, the Examiner asserts that the recitation "establishing a bound on the execution time of an application due to task interference in a shared instruction cache" has not been given patentable weight because the recitation occurs in the preamble. The Examiner further asserts that the broadest reasonable interpretation of a live cache frame is "merely a data block in cache" and that the specification does not contradict this broadest reasonable interpretation of the claim.

Applicants note that Kikuchi is directed to "a device control apparatus and a control method for forming protection data such as a CRC or the like and adding it when user data from an upper apparatus such as a host or the like is buffered into a cache memory." (Col. 1, lines 12-16). Applicants also note that Kikuchi teaches a case

> where the transfer is interrupted in association with the path switching of the fabric 12. In this state, the transfer of the data block and the formation of the protection data cannot be simultaneously performed. On the other hand, in the RAID controllers 18-1 to 18-3 of the invention, a fact that the *transfer of the data*

> *block was interrupted is detected during the transfer of the user data from the host and a state of the forming circuit of the protection data at that time is stored. After that, when the restart of the transfer of the data block is detected, the state is returned to the stored circuit state upon interruption and the formation of the protection data is restarted.*"
> (Col. 6, lines 47-59; emphasis added.)

Kikuchi, however, does ***not*** address the issue of establishing a bound on the execution time of an application due to task interference in a shared instruction cache, as required by the claims of the present invention. Regarding the Examiner's assertion that the recitation "establishing a bound on the execution time of an application due to task interference in a shared instruction cache" has not been given patentable weight because the recitation occurs in the preamble, Applicants note that Applicants' argument does not strictly rely on this feature to overcome the cited prior art. Applicants also note, however, that the body of the cited claims require "establishing said bound," and that the preamble recites that the bound is "on the execution time of an application due to task interference in a shared instruction cache." Thus, since the preamble provides completeness for the body of the claims, the preamble should be given patentable weight.

Applicants also note that the present disclosure defines "live cache frames" as, for example, "a cache frame that contains a *block that is accessed in the future without an intervening eviction.* The present invention recognizes that the eviction of blocks from a live frame by an interrupt causes a future miss that would not otherwise occur and that evictions from live frames are the only evictions that cause misses that would not otherwise occur." (Page 2, lines 19-22; emphasis added.)

Clearly, a patentee is entitled to be his own lexicographer. See, e.g., *Rohm & Haas Co. v. Dawson Chemical Co., Inc.*, 557 F. Supp 739, 217 U.S.P.Q. 515, 573 (Tex. 1983); *Loctite Corp. v. Ultraseal Ltd.*, 781 F.2d 861, 228 U.S.P.Q. 90 (Fed. Cir. 1985); and *Fonar Corp. v. Johnson & Johnson*, 821 F.2d 627, 3 U.S.P.Q.2d 1109 (Fed. Cir. 1987).

The interpretation of the term "live cache frame" asserted by the Examiner is inconsistent with the definition provided in the specification and is not how the term would be understood by a person of ordinary skill, based on the specification. When the specification

explains and defines a term used in the claims, without ambiguity or incompleteness, there is no need to search further for the meaning of the term. *Multiform Desiccants Inc. v. Medzam Ltd.*, 133 F.3d 1473, 45 U.S.P.Q.2d 1429, 1433 (Fed. Cir. 1998).

Applicants could find no disclosure or suggestion by Kikuchi of live frames, of determining *a number of live frames* of said application that are *coexistent during execution* of said application; and of *establishing a bound based on the number of live frames*. Independent claims 1, 7, 13, and 16 require determining a number of live frames of said application that are coexistent during execution of said application; and establishing said bound based on said number of live frames.

Thus, Kikuchi does not disclose or suggest determining a number of live frames of said application that are coexistent during execution of said application; and establishing said bound based on said number of live frames, as required by independent claims 1, 7, 13, and 16.

Additional Cited References

Borg et al. was also cited by the Examiner for its disclosure of a cache simulation routine to analyze memory access patterns of a cache. Applicants note that Borg is directed to utilizing "link time code modification to instrument the code which is to be executed, typically comprising plurality of kernel operations and user programs." (See, Abstract.) Applicants could find no disclosure or suggestion by Borg et al. of live frames, of determining *a number of live frames* of said application that are *coexistent during execution* of said application; and of *establishing a bound based on the number of live frames*.

Thus, Borg et al. do not disclose or suggest determining a number of live frames of said application that are coexistent during execution of said application; and establishing said bound based on said number of live frames, as required by independent claims 1, 7, 13, and 16.

Hwu et al. was also cited by the Examiner for its disclosure of detecting and monitoring usage patterns of the data elements in a cache line after access (col. 3, lines 27-54). Applicants note that Hwu is directed to detecting and monitoring program hot spots during execution that may be implemented in hardware. (See, Abstract.) Applicants could find no disclosure or suggestion by Hwu et al. of live frames, of determining *a number of live frames* of said application that are *coexistent during execution* of said application; and of *establishing a*

bound based on the number of live frames.

Thus, Hwu et al. do not disclose or suggest determining a number of live frames of said application that are coexistent during execution of said application; and establishing said bound based on said number of live frames, as required by independent claims 1, 7, 13, and 16.

Dependent Claims 2-6, 8-12, 14-15 and 17-20

Dependent claims 2, 5, 8, 11, 14, and 19 were rejected under 35 U.S.C. §102(e) as being anticipated by Kikuchi, claims 3, 9, and 17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kikuchi in view of Hwu et al., and claims 4, 6, 10, 12, 15, 18, and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kikuchi in view of Borg et al.

Claims 2-6, 8-12, 14-15, and 17-20 are dependent on claims 1, 7, 13, and 16, respectively, and are therefore patentably distinguished over Kikuchi, Hwu et al., and Borg et al., alone or in combination, because of their dependency from independent claims 1, 7, 13, and 16 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims, i.e., claims 1-20, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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